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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,305	12/16/2003	Kassem M. Abdallah	EMC-03-104	5962

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,305	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,13-17,25 and 28-31 is/are rejected.

7)☒ Claim(s) 5-12,18-24,26 and 27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 28-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 28, the relationships between the steps are unclear/ambiguous. In particular, step A is directed to processing access indication signals received from each of the plurality of processors whereas step D is directed to receiving an access indication signal from a particular one of the plurality of processors. It is not ascertained how the step of processing can be performed before the step of receiving. Further, the term "an access arbitration signal" used in step C and E cannot be ascertained. In step E, the language "arbitrating access to the particular processor" is not understood. Claim 28 is directed to a method for arbitrating access to a shared resource.

In claim 29, the language "granting access to the shared resource by the particular processor" is not understood. The arbiter is used to grant access to the shared recourse, not the processor.

In claim 30, the language "blocking access to the shared resource by the particular processor" is not understood. The arbiter is used to block or deny access to the shared recourse, not the processor.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 13-17, 25, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Derrick et al.

As broadly drafted, these claims do not define any structure/step that differs from Derrick et al. (Derrick, 5,782,980).

With regard to claim 1, Derrick discloses a system for arbitrating access to a shared resource (shown generally at Fig. 4) comprising:

a plurality of microprocessors (406, see also col. 1, lines 22-27 and 31-43); a shared resource (408, Fig. 4 or 706, Fig. 7); and a controller (402, Fig. 4 or 710, Fig. 7) coupled to the plurality of microprocessors (406, see also col. 1, lines 22-27 and 31-43) and the shared resource (408, Fig. 4 or 706, Fig. 7) by a first bus (bus 404 connecting the bus masters to the bus controller 402; or local bus 704, Fig. 7) and a second bus (the bus connecting the shared resource to the bus controller as shown in Fig. 4 or the bus connecting the system memory 706 to the controller 710 as shown in Fig. 7), respectively, the controller (402, Fig. 4 or 710, Fig. 7) including a register (spin buffer

502 of the controller 710, for example, includes at least one register 520) having a lock portion associated with each of the plurality of processors (ID field associated with each of the plurality of masters/processors, see at least col. 5, lines 2-51) and at least one status portion (field containing 1 bit LOCK, see at least col. 5, lines 2-51), each of the lock portions (ID field associated with each of the plurality of masters/processors) indicating whether the associated one of the plurality of microprocessors has obtained access to communicate with the shared resource (see at least col. 5, line 2 to col. 6, line 53) and each of the at least one status portions (field containing 1 bit LOCK) includes a bit indicating whether any of the plurality of microprocessors has obtained access to communicate with the shared resource (see at least col. 5, line 2 to col. 6, line 53).

With regard to claim 2, it is clear that the shared resource comprises a memory device such as memory 706.

With regard to claim 3, it is clear that the system of Derrick includes includes a plurality of shared resources (see at least Fig. 4).

With regard to claim 4, it is clear that the register includes at least as many lock portions and status portions as there are shared resources, wherein each shared resource has a lock portion and a status portion associated therewith (see at least Fig. 5 and description thereof; see also col. 5, line 2 to col. 6, line 53).

With regard to claim 13, Derrick discloses a controller (shown generally at Figs. 4-7) for arbitrating access to at least one shared resource (408/706) by a plurality of processors (406, see also col. 1, lines 22-27 and 31-43), the controller comprising: a first register portion (registers used for "ID" included in spin buffer 502, Fig. 5, for

example) including a plurality of layers (a plurality of stacked registers), each of the plurality of layers being associated with a different one of the plurality of processors (406, see also col. 1, lines 22-27 and 31-43), each of the plurality of layers (a plurality of registers 520) including an access indication portion (ID filed, see at least col. 5, lines 2-51) associated with each of the at least one shared resource (408/706), the access indication portion (ID filed, see at least col. 5, lines 2-51) holding an indicator (M bits) of whether a processor (406, see also col. 1, lines 22-27 and 31-43) associated with a particular layer (a plurality of registers) has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer (see at least col. 5, lines 2-51); and an access arbitration device (arbiter 506, Fig. 5/arbitration logic, Fig. 4), for example) associated with all of the access indication portions (of spin buffer 502 associated with arbiter 506, Fig. 5/arbitration logic, Fig. 4) of each of the at least one shared resources (408/706) for controlling access to the associated shared resource (408/706) by the plurality of processors (406, see also col. 1, lines 22-27 and 31-43), the access arbitration device (arbiter 506, Fig. 5/arbitration logic, Fig. 4, for example) including an input for receiving access indication signals from the plurality of processors (it is clear that the so-called "access indication signals" from the masters/processors must be received by the arbiter before arbitration can be performed), the access arbitration device: (A) determining whether the at least one shared resource is being accessed by any of the plurality of processors (the arbiter must first determine whether the shared resource is free before granting access to one of the masters/processors); and (B) arbitrating access to the shared resource based on

the determination made Step (A) (it is clear that if the shared resource is determined to be free then arbitration can be performed by the arbiter employing an arbitration logic).

With regard to claim 14, in Derrick, if a particular processor of the plurality of processors ((406, see also col. 1, lines 22-27 and 31-43) requires access to a particular one of the at least one shared resources (408/706), it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, no other processor has access to the shared resource, as determined in Step (A) ((the arbiter must first determine whether the shared resource is free before granting access to one of the masters/processors), the access arbitration device grants access to the particular shared resource by the particular processor (it is clear that if the shared resource is determined to be free then arbitration can be performed by the arbiter employing an arbitration logic).

With regard to claim 15, in Derrick, if a particular processor of the plurality of processors requires access to a particular one the at least one shared resources, it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, if another processor has access to the shared resource, as determined in Step (A), the access arbitration device denies access to the particular shared resource by the particular processor (it is clear that if a shared resource is accessed by a particular master/processor, then the arbiter denies access to the shared resource; arbitration among masters/processors is performed only when the shared resource is free or available for accessing).

With regard to claim 16, in Derrick, the access arbitration device grants access to the particular shared resource by the particular processor by passing the access indicator input to the access arbitration device by the particular processor to the access indication portion for the particular shared resource in the layer associated with the particular processor (if a particular master/processor gains access to the shared resource via arbitration, the LOCK bit is set in the registers of the spin buffer).

With regard to claim 17, in Derrick, it is clear that the access arbitration device denies access to the particular shared resource by the particular processor by clearing the access indicator input to the access arbitration device by the particular processor (when the shared resource is not available, the request for access to the shared resource of a particular master/processors is denied, and according to the principle of arbitration, the master/processor must retry, or in other words, the access indicator input to the access arbitration device by the particular processor is cleared by a new access indicator input to the access arbitration device by the particular processor must provided to the arbiter for arbitration for access to the shared resource.

With regard to claim 25, the controller of Derrick further comprises a second register portion (registers for "LOCK" included in spin buffer 502) including a status indication portion (LOCK bit) associated with each of the at least one shared resources, each status indication portion including a status indicator which indicates whether the shared resource associated with the status indication portion is being accessed by one of the plurality of processors (see at least col. 5, lines 2-51).

With regard to claims 28-31, as best the Examiner can ascertain from the language of the claims, these claims do not define any step that differs from Derrick. See discussion above. Note also that the term "access arbitration signal" used in step C and step D are understood as a signal for indicating to the arbiter that whether the shared recourse is free or available so that arbitration for access to the shared resource can be performed based on whether the shared recourse is free or available.

Allowable Subject Matter

Claims 5-12, 18-24, 26, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

U.S. Patent Nos. 4,574,350 to Starr, 5,935,234 to Arimilli et al., 5,341,491 to Ramanujan, and 5,175,837 to Arnold are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner